performing a first RTA (Rapid Thermal Annealing) process to form a first-reacted silicide region;

providing a supplemental silicon layer over the surface of the semiconductor device, including the first-reacted silicide region; and

performing a second RTA process to convert the first-reacted silicide region into [form] a second-reacted silicide region, by reaction of the supplemental silicon layer ~~with the first-reacted silicide region.~~

2. (Amended) [A] The method according to claim 1, wherein the material comprises cobalt (Co).

3. (Amended) [A] The method according to claim 1, wherein the material comprises titanium (Ti).

4. (Amended) [A] The method according to claim 1, wherein the supplemental silicon layer is [of] poly-silicon formed by a CVD (Chemical Vapor Deposition) technique.

5. (Amended) [A] The method according to claim 1, wherein the supplemental silicon layer is [of] a-Si [(amorphousness] (amorphous silicon) formed by a sputtering technique.

6. (Amended) [A] The method according to claim 1, further comprising [the step of]:

selectively removing non-reacted silicon from the second-reacted silicide region ~~after the second RTA process.~~

~~7. (Amended) [A] The method according to claim 1, further comprising [the step of]:~~

doping an impurity into the supplemental silicon layer before the second RTA process, wherein the impurity is of [the] a same type as active regions formed in the surface of the semiconductor device.

8. (Amended) [A] The method according to claim 7, wherein the impurity is doped into one of an N-channel region and a P-channel region.

9. (Amended) A method for fabricating a semiconductor device using a salicide (self aligned silicide) process, comprising [the steps of]:

providing a silicon substrate;

providing a BOX (Buried Oxide) layer [in] on the silicon substrate;

providing a [filed] field oxide layer and [a] an SOI (Silicon on Insulator) layer on the BOX layer;

providing a gate oxide layer on the SOI layer;

providing a poly-silicon gate layer on the gate oxide layer;

providing a gate side wall layer on the SOI layer to surround the poly-silicon gate layer and the gate oxide layer;

providing a material to be silicided on [the] a surface of the semiconductor device including the poly-silicon gate layer, the gate side wall layer, the SOI layer and the field oxide layer;

performing a first RTA (Rapid Thermal Annealing) process to form first-reacted silicide regions in the poly-silicon gate layer and in source/drain active areas of the SOI layer;

removing non-reacted material from the first-reacted silicide regions;

providing a supplemental silicon layer over the [entire] surface of the semiconductor device after the non-reacted material is removed;

performing a second RTA process to convert [so that] the first-reacted silicide regions into second-reacted silicide regions, by reaction of [react again with] the supplemental silicon layer [to form second-reacted] with the first-reacted silicide regions; and

~~selectively removing non-reacted silicon from the second-reacted silicide regions.~~

Please add new claims 19-22 as follows:

--19. The method according to claim 1, wherein the first-reacted silicide region is formed to extend into the surface of the semiconductor device.

20. The method according to claim 1, wherein the surface of the semiconductor

device comprises a substrate, a buried oxide layer formed on the substrate and a silicon-on-insulator layer formed on the buried oxide layer,

the first RTA process comprising forming the first-reacted silicide region as extending into the silicon-on-insulator layer.

21. The method according to claim 1, further comprising removing the material after the first RTA process prior to the providing of the supplemental silicon layer.

22. The method according to claim 9, wherein said providing a field oxide layer and an SOI layer on the BOX layer comprises providing the SOI layer as having an amount of silicon so that the first-reacted silicide regions are completely formed during said first RTA process and so that an appropriate amount of the silicon remains in the ~~SOI layer after said second RTA process.~~

REMARKS

Claims 1-9 and 19-22 are pending in the present application. Claims 19-22 have been presented herewith.

Priority Under 35 U.S.C. 119

The Examiner has acknowledged a Claim for Foreign Priority under 35 U.S.C. 119 in the current Office Action dated July 18, 2000. **However, a claim for foreign**